FIG.1

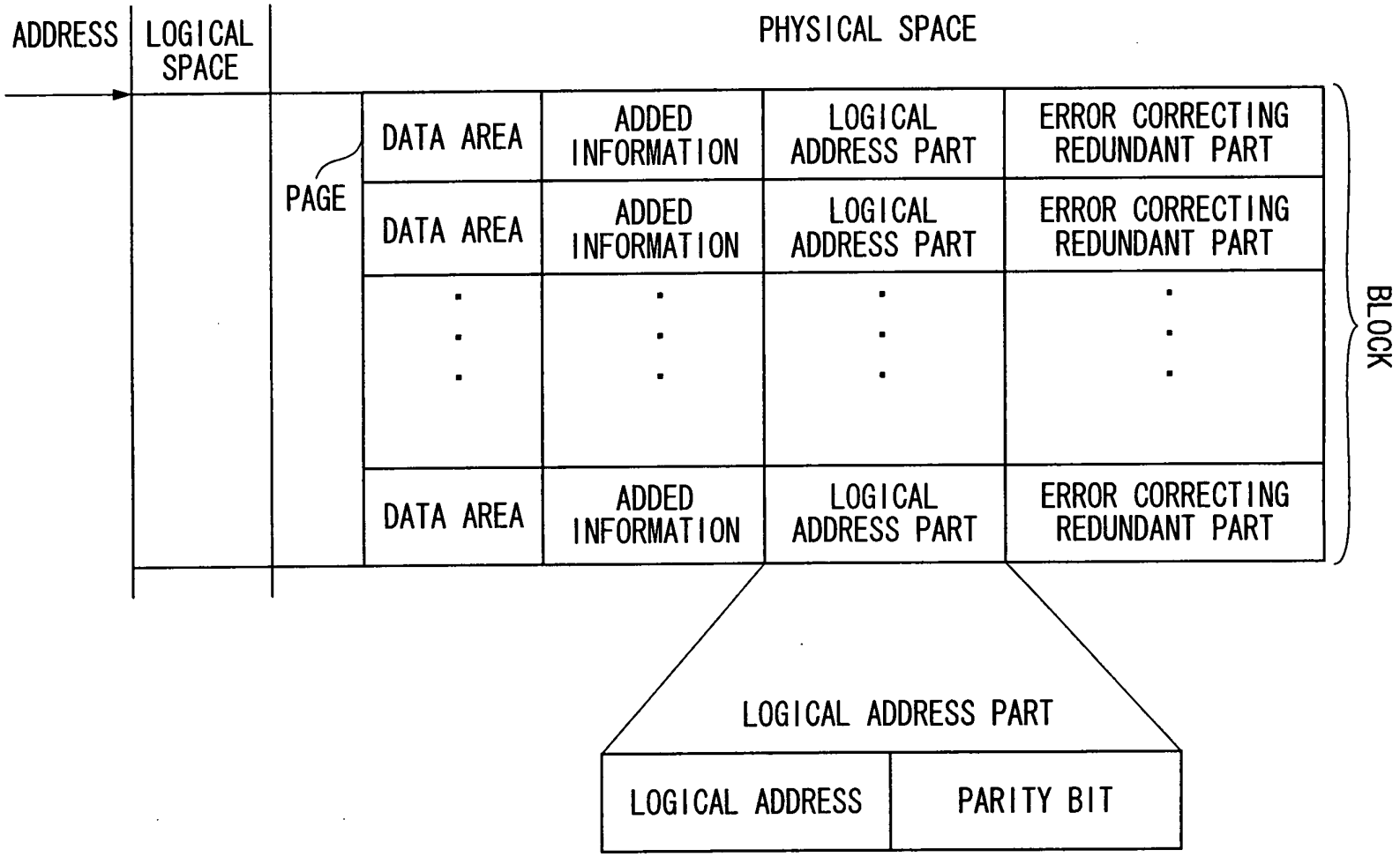

ADDRESS
LOGICAL SPACE
PHYSICAL SPACE
PAGE
DATA AREA
ADDED INFORMATION
LOGICAL ADDRESS PART
ERROR CORRECTING REDUNDANT PART
DATA AREA
ADDED INFORMATION
LOGICAL ADDRESS PART
ERROR CORRECTING REDUNDANT PART
DATA AREA
ADDED INFORMATION
LOGICAL ADDRESS PART
ERROR CORRECTING REDUNDANT PART
BLOCK
LOGICAL ADDRESS PART
LOGICAL ADDRESS
PARITY BIT

FIG.2

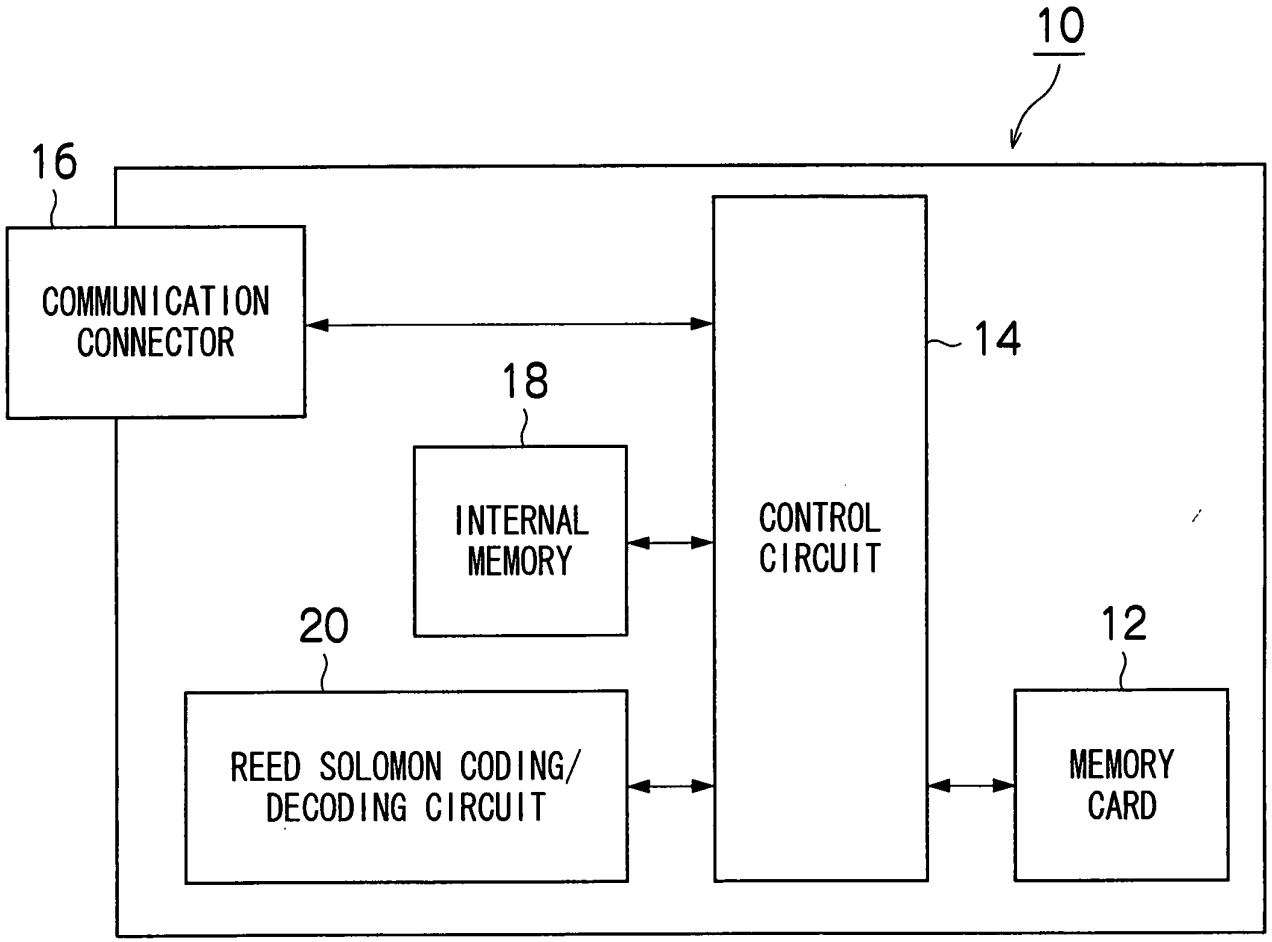

10
16
COMMUNICATION CONNECTOR
18
INTERNAL MEMORY
CONTROL CIRCUIT
14
20
REED SOLOMON CODING/ DECODING CIRCUIT
12
MEMORY CARD

FIG.3

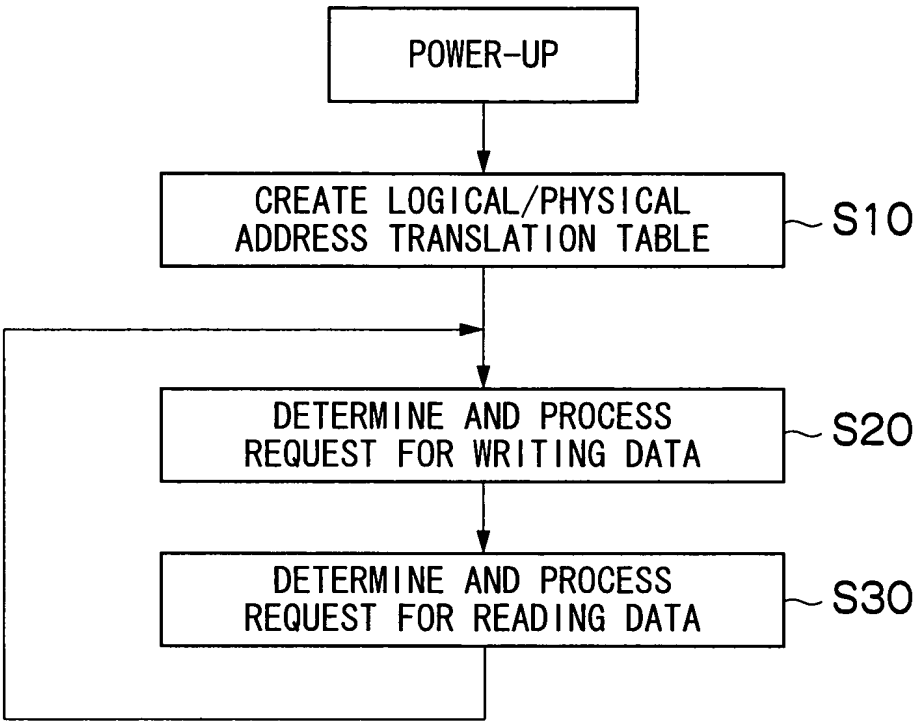

POWER-UP
CREATE LOGICAL/PHYSICAL ADDRESS TRANSLATION TABLE
S10
DETERMINE AND PROCESS REQUEST FOR WRITING DATA
S20
DETERMINE AND PROCESS REQUEST FOR READING DATA
S30

FIG.4

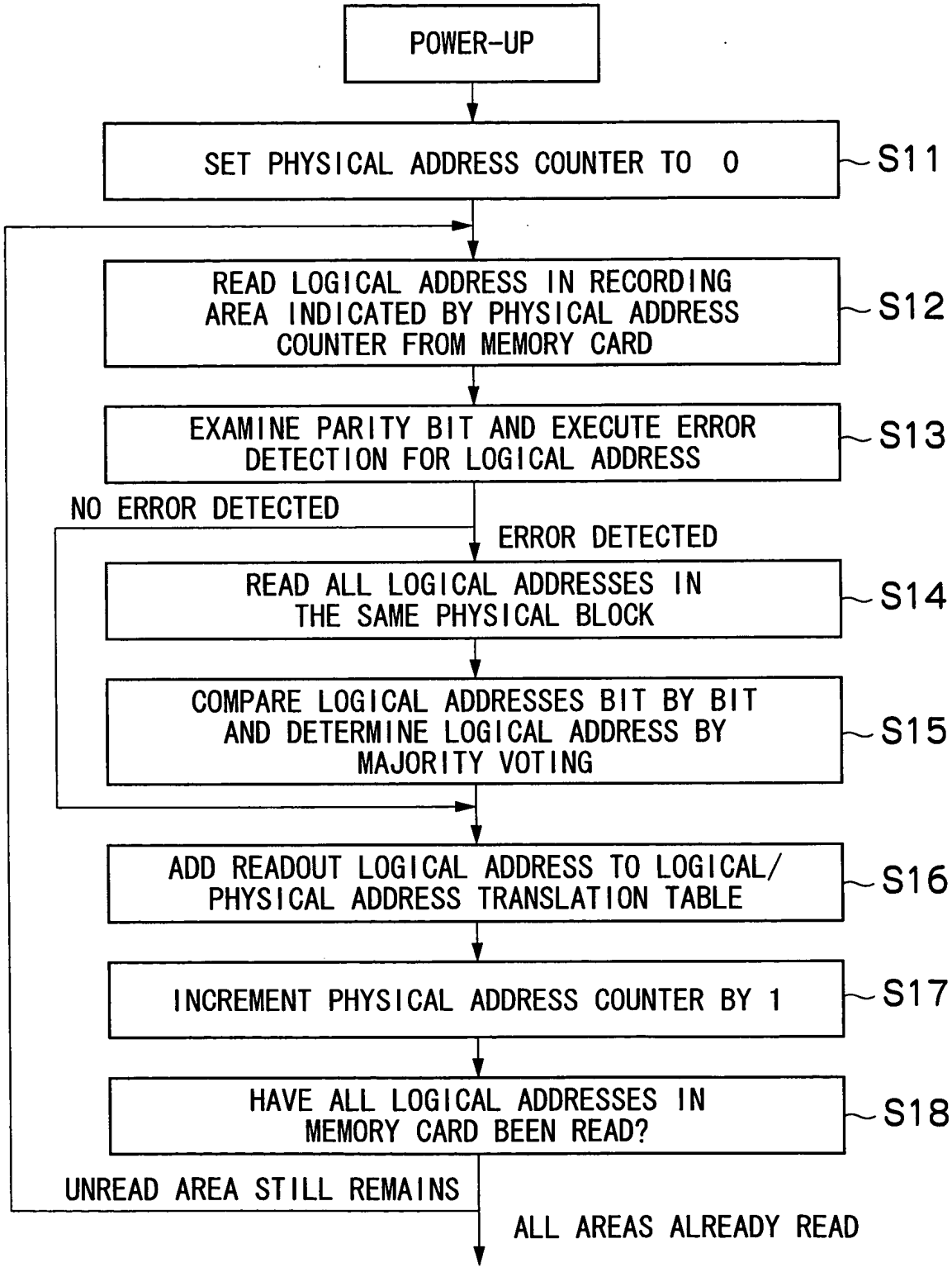

POWER-UP
SET PHYSICAL ADDRESS COUNTER TO 0
S11
READ LOGICAL ADDRESS IN RECORDING AREA INDICATED BY PHYSICAL ADDRESS COUNTER FROM MEMORY CARD
S12
EXAMINE PARITY BIT AND EXECUTE ERROR DETECTION FOR LOGICAL ADDRESS
S13
NO ERROR DETECTED
ERROR DETECTED
READ ALL LOGICAL ADDRESSES IN THE SAME PHYSICAL BLOCK
S14
COMPARE LOGICAL ADDRESSES BIT BY BIT AND DETERMINE LOGICAL ADDRESS BY MAJORITY VOTING
S15
ADD READOUT LOGICAL ADDRESS TO LOGICAL/ PHYSICAL ADDRESS TRANSLATION TABLE
S16
INCREMENT PHYSICAL ADDRESS COUNTER BY 1
S17
HAVE ALL LOGICAL ADDRESSES IN MEMORY CARD BEEN READ?
S18
UNREAD AREA STILL REMAINS
ALL AREAS ALREADY READ

FIG.5

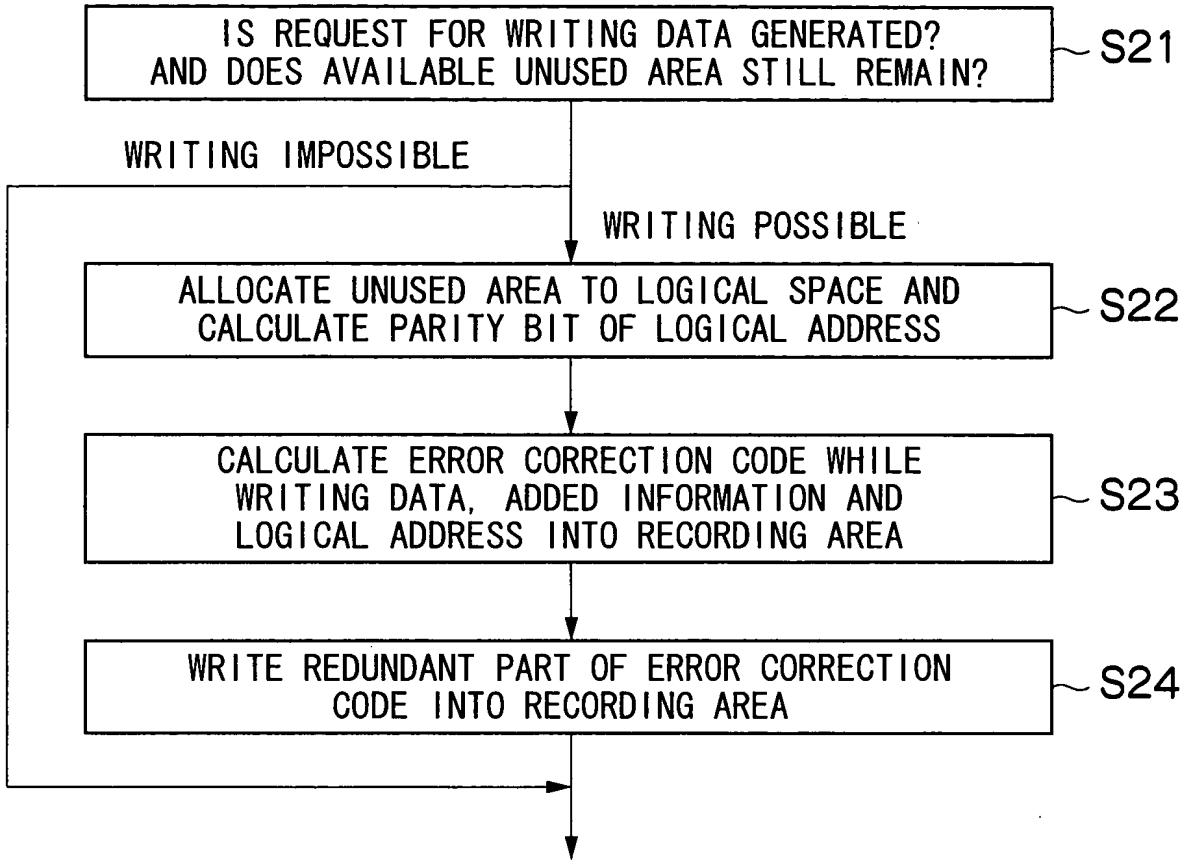
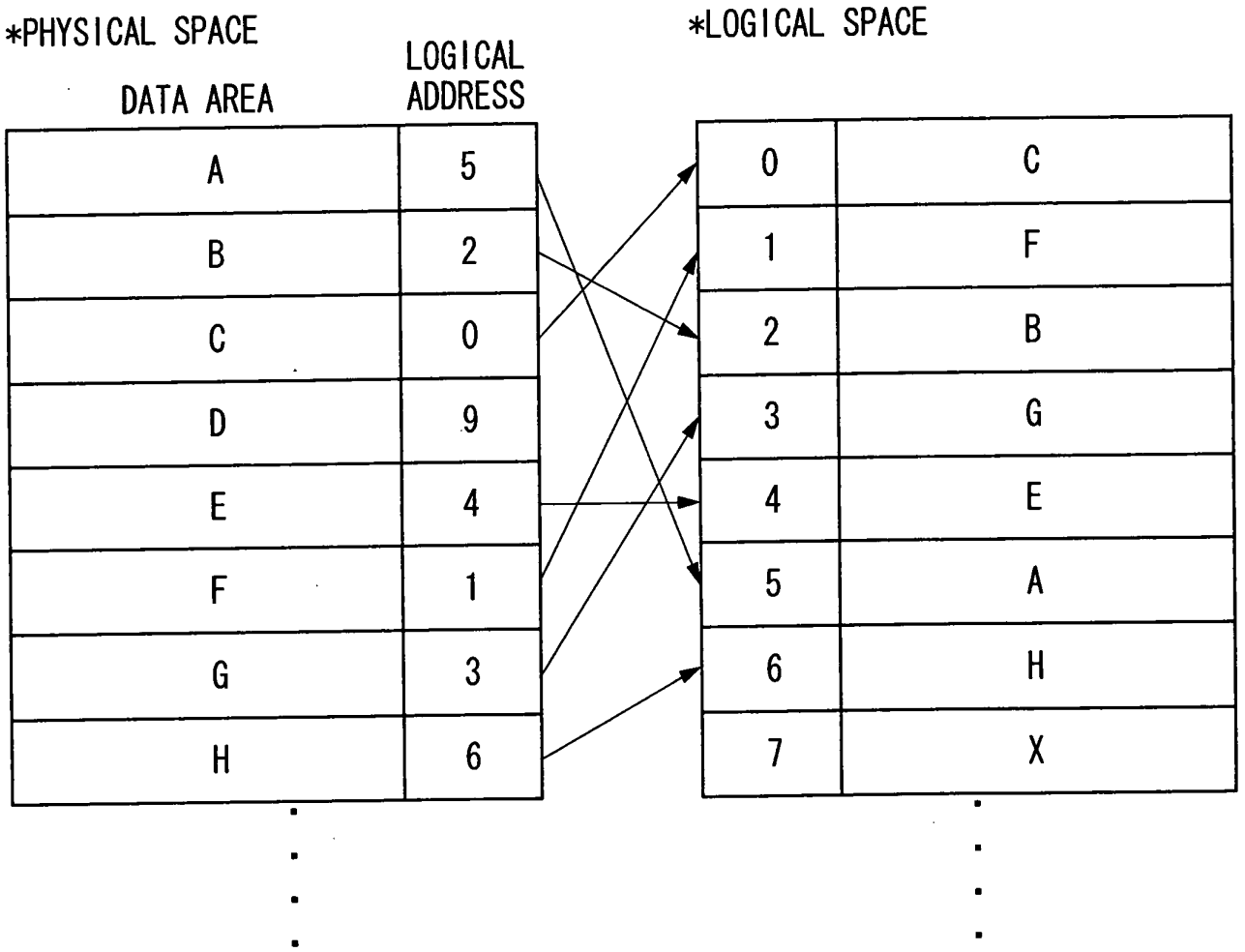
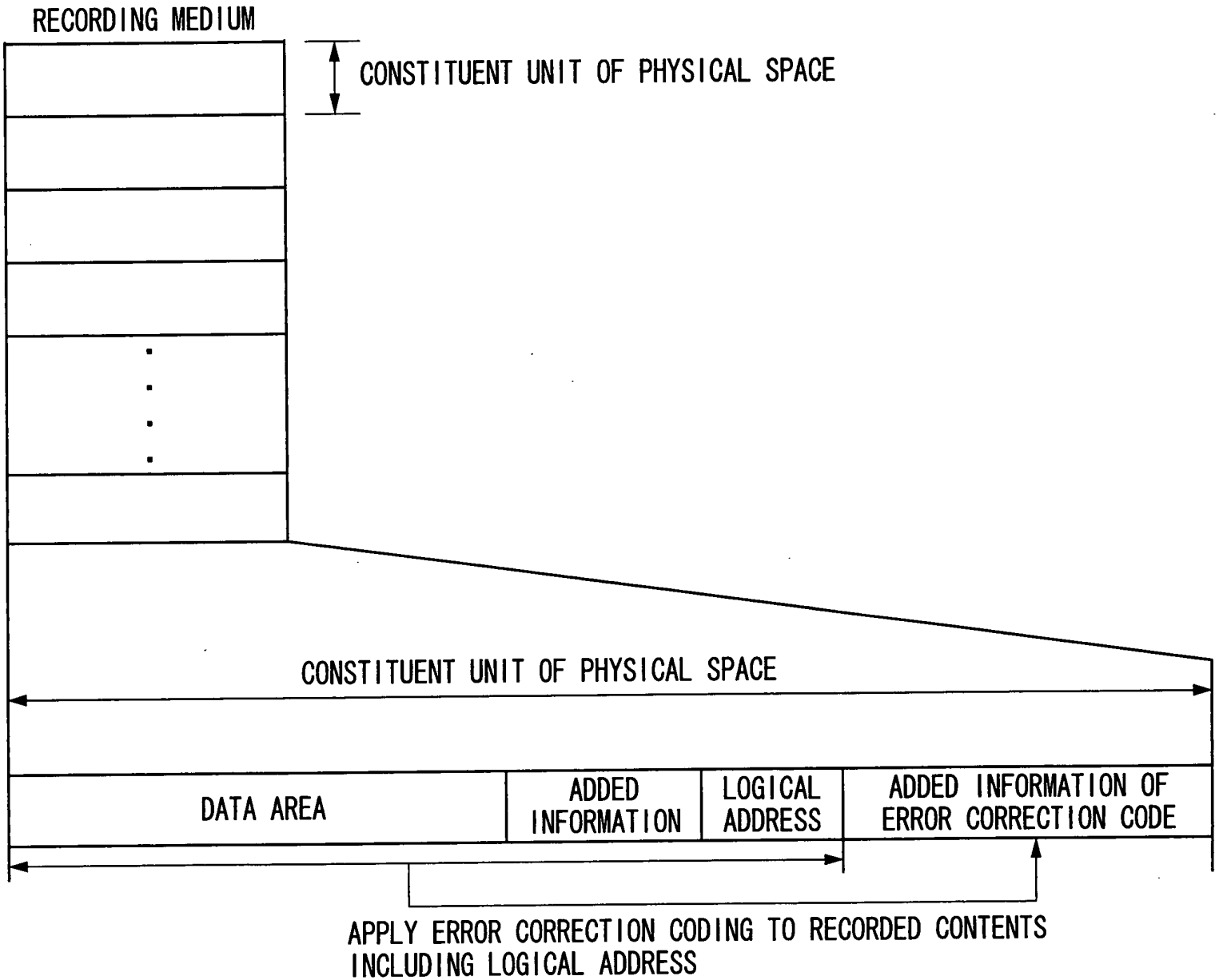

IS REQUEST FOR WRITING DATA GENERATED?
AND DOES AVAILABLE UNUSED AREA STILL REMAIN?
S21
WRITING IMPOSSIBLE
WRITING POSSIBLE
ALLOCATE UNUSED AREA TO LOGICAL SPACE AND
CALCULATE PARITY BIT OF LOGICAL ADDRESS
S22
CALCULATE ERROR CORRECTION CODE WHILE
WRITING DATA, ADDED INFORMATION AND
LOGICAL ADDRESS INTO RECORDING AREA
S23
WRITE REDUNDANT PART OF ERROR CORRECTION
CODE INTO RECORDING AREA
S24

FIG.6
PRIOR ART



ALLOCATION FROM PHYSICAL SPACE TO LOGICAL SPACE USING LOGICAL ADDRESS

FIG.7


RECORDING MEDIUM
CONSTITUENT UNIT OF PHYSICAL SPACE
CONSTITUENT UNIT OF PHYSICAL SPACE
DATA AREA
ADDED INFORMATION
LOGICAL ADDRESS
ADDED INFORMATION OF ERROR CORRECTION CODE
APPLY ERROR CORRECTION CODING TO RECORDED CONTENTS INCLUDING LOGICAL ADDRESS